Notice of Allowability	Application No. 10/724,277	Applicant(s) MCGAUGHY ET AL.	
	Examiner Shambhavi Patel	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *8/4/06*.

2. ☒ The allowed claim(s) is/are *1-21*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 6/21/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. The amendment filed 4 August 2006 has been received and considered. Claims 1-21 have been presented for examination.

Remarks

2. **The 35 U.S.C. 101 and 112 1st and 2nd rejections have been withdrawn** subsequent to Applicant's persuasive arguments.

Response to Arguments

3. Applicant's arguments, see pages 14-16, filed 04 August 2006, with respect to claims1-21 have been fully considered and are persuasive. The rejection of claims 1-21 has been withdrawn. The Examiner notes that the meaning of the term 'dynamic database' is interpreted as specifically disclosed on page 11 of the specifications, and that the dynamic database must allow for dynamic merging and/or splitting of the circuits, as disclosed in paragraphs [0037]-[0039] of the specification.

Examiner's Amendment

4. **An examiner's amendment to the record appears below.** Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Please amend paragraph **[0001]** of the specification as follows:

> [0001] This application is related to the following U.S. Patent applications, each of which is hereby incorporated by reference in its entirety: System and Method for Dynamically Compressing Circuit Components During Simulation, Serial No. 10/713,729, filed November 13, 2003, currently pending; System and Method for Adaptive Partitioning of Circuit Components During Simulation, US Patent No. 7,024,652; System and Method

for Communicating Simulation Solutions Between Circuit Components in a Hierarchical Data Structure, Serial No. 10/713,754, filed November 13, 2003, currently pending; System and Method for Supporting Multi-Rate Simulation of a Circuit Having Hierarchical Data Structure, Serial No. 10/713,753, filed November 13, 2003, currently pending; and System and Method for Dynamically Representing Repetitive Loads of a Circuit During Simulation, Serial No. 10/713,728, filed November 13, 2003, currently pending.

Allowable Subject Matter

5. **Claims 1-21 are allowed**. The following is an examiner's **statement of reasons for allowance**:

Regarding claim 1:

The **prior art of record discloses** a method of simulating a circuit having a hierarchical data structure, comprising representing the circuit as a hierarchically arranged set of branches, including a root branch and a plurality of other branches logically organized in a graph; the hierarchically arranged set of branches including a first branch that includes one or more leaf circuits and a second branch that includes one or more leaf circuits; wherein the first branch and second branch are interconnected in the graph through a third branch at a higher hierarchical level in the graph than the first and second branches; creating a static database in accordance with a netlist description of the circuit, the static database including topology information of the circuit; selecting a group circuit for simulation, the group circuit comprises one or more leaf circuits selected from the first branch and the second branch.

However, **the prior art does not teach or suggest** creating a dynamic database for representing the group circuit, the dynamic database including references to corresponding branches of the hierarchical data structure in the static database for fetching topology information dynamically during the simulation, and simulating the group circuit in accordance with the dynamic database. The Examiner notes that the

meaning of the term *'dynamic database'* is interpreted as specifically disclosed on page 11 of the specifications, and that the dynamic database must allow for dynamic merging and/or splitting of the circuits, as disclosed in paragraphs [0037]-[0039] of the specification. The Examiner further notes that the 'dynamic isomorphic partitioning' taught in paragraphs [0037]-[0039] of the specification appears to directed to reducing the number of cells to be processed by identifying and combining circuits displaying identical behavior.

Furthermore, the prior art of record does not meet the conditions as suggested in MPEP section 2132, namely:

"The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an **ipsissimis verbis** test, i.e., identity of terminology is not required. **In re Bond**, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."

In particular, the **prior art of record does not disclose the specific sequence of method steps inclusive of** "simulating a circuit having a hierarchical data structure, comprising representing the circuit as a hierarchically arranged set of branches, including a root branch and a plurality of other branches logically organized in a graph; the hierarchically arranged set of branches including a first branch that includes one or more leaf circuits and a second branch that includes one or more leaf circuits; wherein the first branch and second branch are interconnected in the graph through a third branch at a higher hierarchical level in the graph than the first and second branches; creating a static database in accordance with a netlist description of the circuit, the static database including topology information of the circuit; selecting a group circuit for simulation, the group circuit comprises one or more leaf circuits selected from the first branch and the second branch; creating a dynamic database for representing the group circuit, the dynamic database including references to corresponding branches of the hierarchical data structure in the static database for fetching topology information dynamically during the simulation, and

simulating the group circuit in accordance with the dynamic database" as now recited in independent claim 1.

Dependent claims 2-7 are deemed allowable as depending from independent claim 1.

Regarding claim 8:

The **prior art of record discloses** a system for simulating a circuit having a hierarchical data structure, comprising at least one processing unit for executing computer programs; a user interface for performing at least one of the functions selected from the group consisting of entering a netlist representation of the circuit, viewing representations of the circuit on a display, and observing simulation results of the circuit; a memory for storing a static database; means for representing the circuit as a hierarchically arranged set of branches, including a root branch and a plurality of other branches logically organized in a graph; the hierarchically arranged set of branches including a first branch that includes one or more leaf circuits and a second branch that includes one or more leaf circuits; wherein the first branch and second branch are interconnected in the graph through a third branch at a higher hierarchical level in the graph than the first and second branches; means for creating a static database in accordance with a netlist description of the circuit, the static database including topology information of the circuit; means for selecting a group circuit for simulation, the group circuit comprises one or more leaf circuits selected from the first branch and the second branch.

However, the **prior art of record does not teach or suggest** means for creating a dynamic database for representing the group circuit, the dynamic database including references to corresponding branches of the hierarchical data structure in the static database for fetching topology information dynamically during the simulation, and means for simulating the group circuit in accordance with the dynamic database. The Examiner notes that the meaning of the term *'dynamic database'* is interpreted as specifically disclosed on page 11 of the specifications, and that the dynamic database must allow for

dynamic merging and/or splitting of the circuits, as disclosed in paragraphs [0037]-[0039] of the specification. The Examiner further notes that the 'dynamic isomorphic partitioning' taught in paragraphs [0037]-[0039] of the specification appears to directed to reducing the number of cells to be processed by identifying and combining circuits displaying identical behavior.

Independent claim 8 further uses "means for" language and is given deference in view of In re Donaldson and interpreted in view of 35 U.S.C. 112 paragraph 6. The "means for" language and the limitations related thereto of claim 8 are interpreted within the scope of enablement as provided within the relative embodiment provided within applicant's specification. In particular, the specific means for limitations as recited in the claims is interpreted as defined by the specifications as follows:

a. means for representing the circuit as a hierarchically arranged set of branches, including a root branch and a plurality of other branches logically organized in a graph; the hierarchically arranged set of branches including a first branch that includes one or more leaf circuits and a second branch that included one or more leaf circuits; wherein the first branch and second branch are interconnected in the graph through a third branch at a higher hierarchical level in the graph than the first and second branches **[0021]; [0024]**

b. means for creating a static database in accordance with a netlist description of the circuit, the static database including topology information of the circuit **[0024]; [0027]; [0030]**

c. means for selecting a group circuit for simulation, the group circuit comprises one or more leaf circuits selected from the first branch and the second branch **[0032]**

d. means for creating a dynamic database for representing the group circuit, the dynamic database including references to the static database for fetching topology information dynamically during simulation **[0024]; [0027]; [0029]; [0030] – [0031]; [0037]-[0039].**

e. means for simulating the group circuit in accordance with the dynamic databases **[0032] – [0045]**

Furthermore, the prior art of record does not meet the conditions as suggested in MPEP section 2132, namely:

"The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an **ipsissimis verbis** test, i.e., identity of terminology is not required. **In re Bond**, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."

In particular, the **prior art of record does not disclose the specific combination of system elements and features inclusive of** "at least one processing unit for executing computer programs; a user interface for performing at least one of the functions selected from the group consisting of entering a netlist representation of the circuit, viewing representations of the circuit on a display, and observing simulation results of the circuit; a memory for storing a static and dynamic database; means for representing the circuit as a hierarchically arranged set of branches, including a root branch and a plurality of other branches logically organized in a graph; the hierarchically arranged set of branches including a first branch that includes one or more leaf circuits and a second branch that includes one or more leaf circuits; wherein the first branch and second branch are interconnected in the graph through a third branch at a higher hierarchical level in the graph than the first and second branches; means for creating a static database in accordance with a netlist description of the circuit, the static database including topology information of the circuit; means for selecting a group circuit for simulation, the group circuit comprises one or more leaf circuits selected from the first branch and the second branch; means for creating a dynamic database for representing the group circuit, the dynamic database including references to corresponding branches of the hierarchical data structure in the static database for fetching topology information dynamically during the simulation, and means for simulating the group circuit in accordance with the dynamic database." as now recited in independent claim 8.

Dependent claims 9-14 are deemed allowable as depending from independent claim 8.

Regarding claim 15:

The **prior art of record discloses** a simulator module for simulating a circuit having a hierarchical data structure, wherein the simulator module is used in conjunction with at least a processing unit, a user interface, and a memory, and the simulator module includes one or more computer programs containing instructions for representing the circuit as a hierarchically arranged set of branches, including a root branch and a plurality of other branches logically organized in a graph; the hierarchically arranged set of branches including a first branch that includes one or more leaf circuits and a second branch that includes one or more leaf circuits; wherein the first branch and second branch are interconnected in the graph through a third branch at a higher hierarchical level in the graph than the first and second branches; creating a static database in accordance with a netlist description of the circuit, the static database including topology information of the circuit; selecting a group circuit for simulation, the group circuit comprises one or more leaf circuits selected from the first branch and the second branch.

However, **the prior art does not teach or suggest** a simulator module including a computer program containing instructions for creating a dynamic database for representing the group circuit, the dynamic database including references to corresponding branches of the hierarchical data structure in the static database for fetching topology information dynamically during the simulation, and simulating the group circuit in accordance with the dynamic database. The Examiner notes that the meaning of the term *'dynamic database'* is interpreted as specifically disclosed on page 11 of the specifications, and that the dynamic database must allow for dynamic merging and/or splitting of the circuits, as disclosed in paragraphs [0037]-[0039] of the specification. The Examiner further notes that the 'dynamic isomorphic partitioning' taught in paragraphs [0037]-[0039] of the specification appears to directed to reducing the number of cells to be processed by identifying and combining circuits displaying identical behavior.

Furthermore, the prior art of record does not meet the conditions as suggested in MPEP section 2132, namely:

"The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an **ipsissimis verbis** test, i.e., identity of terminology is not required. **In re Bond**, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."

In particular, the **prior art of record does not disclose the specific combination of system elements and features inclusive of** "a simulator module for simulating a circuit having a hierarchical data structure, wherein the simulator module is used in conjunction with at least a processing unit, a user interface, and a memory, and the simulator module includes one or more computer programs containing instructions for representing the circuit as a hierarchically arranged set of branches, including a root branch and a plurality of other branches logically organized in a graph; the hierarchically arranged set of branches including a first branch that includes one or more leaf circuits and a second branch that includes one or more leaf circuits; wherein the first branch and second branch are interconnected in the graph through a third branch at a higher hierarchical level in the graph than the first and second branches; creating a static database in accordance with a netlist description of the circuit, the static database including topology information of the circuit; selecting a group circuit for simulation, the group circuit comprises one or more leaf circuits selected from the first branch and the second branch; creating a dynamic database for representing the group circuit, the dynamic database including references to corresponding branches of the hierarchical data structure in the static database for fetching topology information dynamically during the simulation, and simulating the group circuit in accordance with the dynamic database" as now recited in independent claim 15.

Dependent claims 16-21 are deemed allowable as depending from independent claim 15.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is (571) 272-5877. The examiner can normally be reached on Monday-Friday, 8:00 am – 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SKP

KAMINI SHAH
SUPERVISORY PATENT EXAMINER